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09/928,207	08/10/2001	Robert MacArthur	EMC01-25(01058)	6994

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EXAMINER	
BONZO, BRYCE P	

ART UNIT	PAPER NUMBER
2114	

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2

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/928,207	MACARTHUR ET AL.	
	Examiner	Art Unit	
	Bryce P Bonzo	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 8/10/01.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-22 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-22 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 10 August 2001 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

NON-FINAL OFFICIAL ACTION

Status of the Claims

Claims 1-6,8,9,11-14,16-18,20-22 are rejected under 35 USC §102.

Claims 7,10,15,19 are rejected under 35 USC §103.

Rejections under 35 USC §102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-6,8,9,11-14,16-18,20-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Brant (United States Patent No.5,708,771).

As per claim 1, Brant discloses:

An electronic system, comprising:

critical circuitry (Figures 1 and 3, item 20; column 7, lines 17-22: the cache is critical);

non-critical circuitry having a first section and a second section (column 7, lines 23-25; gray shaded objects; Figure 4, Two controllers are present); and

a power sub-system having a first power assembly, a second power assembly, and a set of connections which is configured to connect the first and second power

assemblies to the critical circuitry and the non-critical circuitry such that, when the first and second power assemblies operate to power the critical and non-critical circuitry through the set of connections (Figure 4, items 48,47,51,52 are powered), (i) a failure of only the second power assembly results in the first power assembly continuing to power the critical circuitry and the first section of the non-critical circuitry (column 9, lines 23-33), and (ii) a failure of only the first power assembly results in the second power assembly continuing to power the critical circuitry and the second section of the non-critical circuitry (column 9, lines 23-33).

As per claim 2, Brant discloses:

The electronic system of claim 1 wherein the first section of the non-critical circuitry includes a first set of storage devices (Figure 3, items 28-32 are disk drives) wherein the second section of the non-critical circuitry includes a second set of storage devices (Figure 3, 23-32 are disk drives, note that Figure 3 is used for both controllers of figure 4), wherein the electronic system operates as a data storage system that stores data into and retrieves data from the first and second sets of storage devices on behalf of a host (column 2, lines 24-27), and wherein the critical circuitry includes cache memory that temporarily buffers data exchanged between the host and the first and second sets of storage devices (column 2, lines 49-55:buffer is a cache).

As per claim 3, Brant discloses:

The electronic system of claim 2 wherein the second set of storage devices is

configured to minor data on the first set of storage devices (4, lines 4-6).

The electronic system of claim 2 wherein the first section of the non-critical circuitry further includes:

a first front-end interface that is configured to operate as an interface between the host and the cache memory(figure 1, item 13: memory controller);, and

a first back-end interface that is configured to operate as an interface between the cache memory and the first set of storage devices (figure 3, item 11, 25,27,29,31 are SCSI);and

wherein the second section of the non-critical circuitry further includes:

a second front-end interface that is configured to operate as an interface between the host and the cache memory (see above), and

a second back-end interface that is configured to operate as an interface between the cache memory and the second set of storage devices (above).

As per claim 5, Brant discloses:

The electronic system of claim 4 wherein the set of connections of the power sub-system includes:

a first interconnect that electrically connects to the first set of storage devices (Figure 1, item 18);

a second interconnect that electrically connects to the second set of storage

devices (Figure 1, item 18 on second controller of figure 4, item 70);

a third interconnect that electrically connects to the cache memory, the first front-end and back-end interfaces, and the second front-end and back-end interfaces (figure 1, 22a, 22b);

a first bus bar assembly that electrically connects the first power assembly to the first and third interconnects (figure 3, item 48); and

a second bus bar assembly that electrically connects the second power assembly to the second and third interconnects (figure 3, item 52).

As per claim 6, Brant discloses:

The electronic system of claim 5 wherein the third interconnect includes:

a backplane having columns of connectors, each column of connectors electrically connecting to one of the first front-end interface, the first back-end interface, the second front-end interface, the second back-end interface (all of the wires of Figure 3, 1, 4 are a backplane)and the cache memory; wherein the first bus bar assembly includes:

a first bus bar that electrically connects the first power assembly to the columns of connectors that electrically connect to the first front-end interface, the first back-end interface and the cache memory without electrically connecting the first power assembly to the columns of connectors that electrically connect to the second front-end interface and the second back-end interface (see claim 5); and

wherein the second bus bar assembly includes:

a second bus bar that electrically connects the second power assembly to the columns of connectors that electrically connect to the second front-end interface, the second back-end interface and the cache memory without electrically connecting to the columns of connectors that electrically connect to the first front-end interface and the first back-end interface (see claim 5).

As per claim 8, Brant discloses:

The electronic system of claim 1, further comprising:

a switch which is interconnected between the first and second power assemblies to voltage balance outputs of the first and second power assemblies (figure 4, items 71-74 combine to form a diode based on/off switch for voltage to the device).

As per claim 9, Brant discloses:

The electronic system of claim 1 wherein the first power assembly of the power sub-system includes:

a first set of main power line connectors to connect to a first main power feed (Figure 4, item 48), and

a first set of auxiliary power line connectors to connect to a first auxiliary power feed (Figure 4, item 47); and

wherein the second power assembly of the power sub-system includes:

a second set of main power line connectors to connect to a second main power feed (Figure 4, item 52), and

a second set of auxiliary power line connectors to connect to a second auxiliary power feed (Figure 4, item 51).

As per claim 11, Brant discloses:

The electronic system of claim 1 wherein the first section of the non-critical circuitry further includes:

a first service processor that provides user access and control to the electronic system (Figure 3, processor 15); and

wherein the second section of the non-critical circuitry further includes:

a second service processor that provides user access and control to the electronic system (Figure 3, Processor 15).

As per claim 12, Brant discloses the power system as shown in the rejection of the electronic system of claim 1 and is rejected on the same grounds.

As per claim 13, Brant discloses the power system as shown in the combined rejection of the electronic system of claims 1-4.

As per claim 14, Brant discloses the power system as shown in the combined rejection of the electronic system of claims 1-4 and 6.

As per claim 16, Brant discloses the power system as shown in the combined rejection of the electronic system of claim 8.

As per claim 17, Brant discloses the power system as shown in the combined rejection of the electronic system of claim 9.

As per claim 18, Brant discloses the method for power as shown in the combined rejection of the electronic system of claim 1.

As per claim 20, Brant discloses the method for power as shown in the combined rejection of the electronic system of claim 1 and 8.

As per claim 21, Brant discloses the method for power as shown in the combined rejection of the electronic system of claim 1 and 9.

As per claim 22, Brant discloses the electronic as shown in the combined rejection of the electronic system of claim 1.

Rejections under 35 USC §103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7, 10, 15 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brant.

As per claim 7, Brant does not disclose:

The electronic system of claim 1 wherein X and Y are integers greater than 0, wherein the first power assembly includes multiple first power supplies that perform a normal operating procedure to provide power to the critical circuitry and to the first section of the non-critical circuitry when up to X first power supplies fail, and an error handling procedure to discontinue providing power to the critical circuitry and to the first section of the non-critical circuitry when more than X first power supplies fail; and wherein the second power assembly includes multiple second power supplies that perform a normal operating procedure to provide power to the critical circuitry and to the second section of the non-critical circuitry when up to Y second power supplies fail, and an error handling procedure to discontinue providing power to the critical circuitry and to the first section of the non-critical circuitry when more than Y second power supplies fail.

Brant does disclose the removal of faulted power supplies. (column 7, lines 4-36). The concept of defining a device as failed when a portion of the device has failed is well known. Thus it would have been obvious to one of ordinary to cease providing power to device when a portion of the power system has failed, thus increasing the

chance that a failure will not propagate through the power system once detected. This creates a more predictable system which is often sought in critical systems.

As per claim 10, Brant does not disclose:

The electronic system of claim 1 wherein the first section of the non-critical circuitry further includes:

a first fan assembly that removes heat from the first section of the non-critical circuitry, and

a second fan assembly that removes heat from the second section of the non-critical circuitry; and

wherein the second section of the non-critical circuitry further includes:

a third fan assembly that removes heat from the first section of the non-critical circuitry, and

a fourth fan assembly that removes heat from the second section of the non-critical circuitry.

Official Notice is taken that the use of multiple fans over circuitry and dedicated to a piece of circuitry is well known in the art. This is down as computer devices generate large amounts of heat, and under high heat, computer devices tend to fail more often. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate multiple fans into the system Brant to ensure fault tolerant operation.

As per claim 15, Brant discloses the power system as shown in the combined rejection of the electronic system of claims 1 and 7.

As per claim 19, Brant discloses the method for power as shown in the combined rejection of the electronic system of claim 1 and 7.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bryce P Bonzo whose telephone number is (703) 305-4834. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Bryce P. Bonzo

Bryce P Bonzo
Examiner
Art Unit 2114

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